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PROVISIONAL APPLICATION COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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2. TITLE OF THE INVENTION

NEW TEST PATTERNS TO COVER RESISTIVE DEFECTS IN THE GLOBAL DATA BUS OF SEMICONDUCTOR MEMORIES

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Respectfully submitted,

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New Test Patterns to Cover Resistive Bridge Defects in the Global Data Bus of Semiconductor Memories

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22 September 2003

Abstract

The invention describes new test patterns to cover resistive bridges at the global read bus and the global write bus in semiconductor memories organized by Z blocks (also known as Z banks). Many techniques have been developed to improve the memory architecture and showed the possibility of including many Z blocks with the same global inputs/outputs. The global read bus and the global write bus play the role of the interface in between the global inputs/outputs and the Z blocks. The data background passes the global inputs/outputs and crosses the global write bus, then reaches the selected Z blocks depending on the address bits. Similarly, The read out data backgrounds passes the sense amplifier and crosses the global read bus, then reaches the global inputs/outputs. From the test point of view, the family of the march test are not sufficient to detect the resistive bridges in between metal lines of the global read bus and the global write bus. The family of these test algorithms comprises of applying insufficient number of data backgrounds to all memory cells that belong to the same memory word. Therefore, the resistive bridges are not completely covered for both the global read/write bus. The invention proposes additional test patterns that have to be applied to the memory to cover the weak points of the family of march test. These new test patterns will enhance the resistive bridges detection at the global read bus and the global write bus and also will cover the entire global paths in semiconductor memories. This solution is based on writing and reading all the data backgrounds needed to cover the resistive bridges. The presented solution in this invention will be generalized also to ROMs and dual port memories (DSRAMs).

1. Problem statement

Nowadays, the architecture of low power and highly densed semiconductor memories is mainly based on multiple Z blocks. Each Z block is divided into different small sub-blocks which are controlled internally from within the Z block. The row address decoder may be divided into three blocks: the pre-decoder, the post-decoder, and internal row decoder which is located internally within the Z block. This internal row decoder selects finally the word line depending on the remainder of the address bits. The selection of determined memory position is done when a determined Z block is activated and when row decoder select a specific rows, and the column decoder selects a specific column. The Z blocks are sharing the global read bus and the global write bus as an interface in between the global inputs/outputs and the matrix.

On the other hand, the family of the march test consists of consecutive read and write with a limited number of data backgrounds which are insufficient to detect the resistive bridges in between the write and read data lines of the global data bus. Therefore, new test patterns are needed to cover the missed defects, otherwise, a test escape will highly impact the customer returns. Using multiple data background

within the family of march test is not feasible, because the complexity of the extended march test will highly depend on the number of bit per word and the memory size. For a memory with B bits per word, a number of $2*(\lceil \log_2 B \rceil + 1)$ data backgrounds are needed to cover all the possible coupling states in between the write data lines and the read data lines of the global data bus. Table 1 shows the data background needed for detecting all these bridging faults for a memory organized by eight bits per word. In fact, the data background needed to test the bus are the same used for detecting the bridging faults in between the memory cells that belong to the same word. However, nowadays this technique is not used anymore because almost all the companies make a word-sliced architecture in which the bits that belong to the same word are not physically adjacent. Many different scrambling are used to distribute the memory cells of the same word through a row. Therefore, the likelihood of a bridging fault in between the memory cells that belong to the same memory word is almost impossible.

Table1: Eight-bit data background to cover bridging faults in the global data bus

Normal
00000000 11111111
01010101 10101010
00110011 11001100
00001111 11110000

Extending the family of the march tests to cover all the data backgrounds shown in Table 1 will explode the complexity of the test algorithm. This solution will highly increase the test time mainly for memory instances with high number of bits per word, and for big memory sizes.

Figure 1 shows a case of a memory with 4 Z blocks and 1024 columns of one bit, each block has it own sense amplifiers, but are sharing the global read bus and the global write bus. A memory may contain until 32 Z Blocks, even more than that for big memories. For instance, suppose a memory with 8 column-slice, 128 bits per word and 32 Z blocks, this means that the memory is 32768 columns of one bit. These columns are distributed from the left corner of the chip to the right corner, and they cover the most area of the memory. Therefore, the global read bus and the global write bus run below all the Z blocks from the left to the right corner of the chip. Thus, the likelihood of having a bridge defect (known as *critical area*) in between the read data lines and the write data lines of the global read/write bus is very high due to the length of the metal and also the space in between one metal line and the neighbours.

The Figure 1 shows a bridge defect in the global read bus (grb) in between the read data lines R[15] and R[14]. This defect will escape the march test when the data backgrounds 00000000 and 11111111 are used. The read and write data lines of the global data bus will drive the same bits (0 or 1) for neighbouring metal lines, therefore the bridge will escape the test. This bridge can be detected if the pattern 01010101 or 10101010 is used as the data background. However, if the neighbouring read and write data lines do not belong to the same metal lines, the bridge will again escape the test with the above-mentioned test patterns.

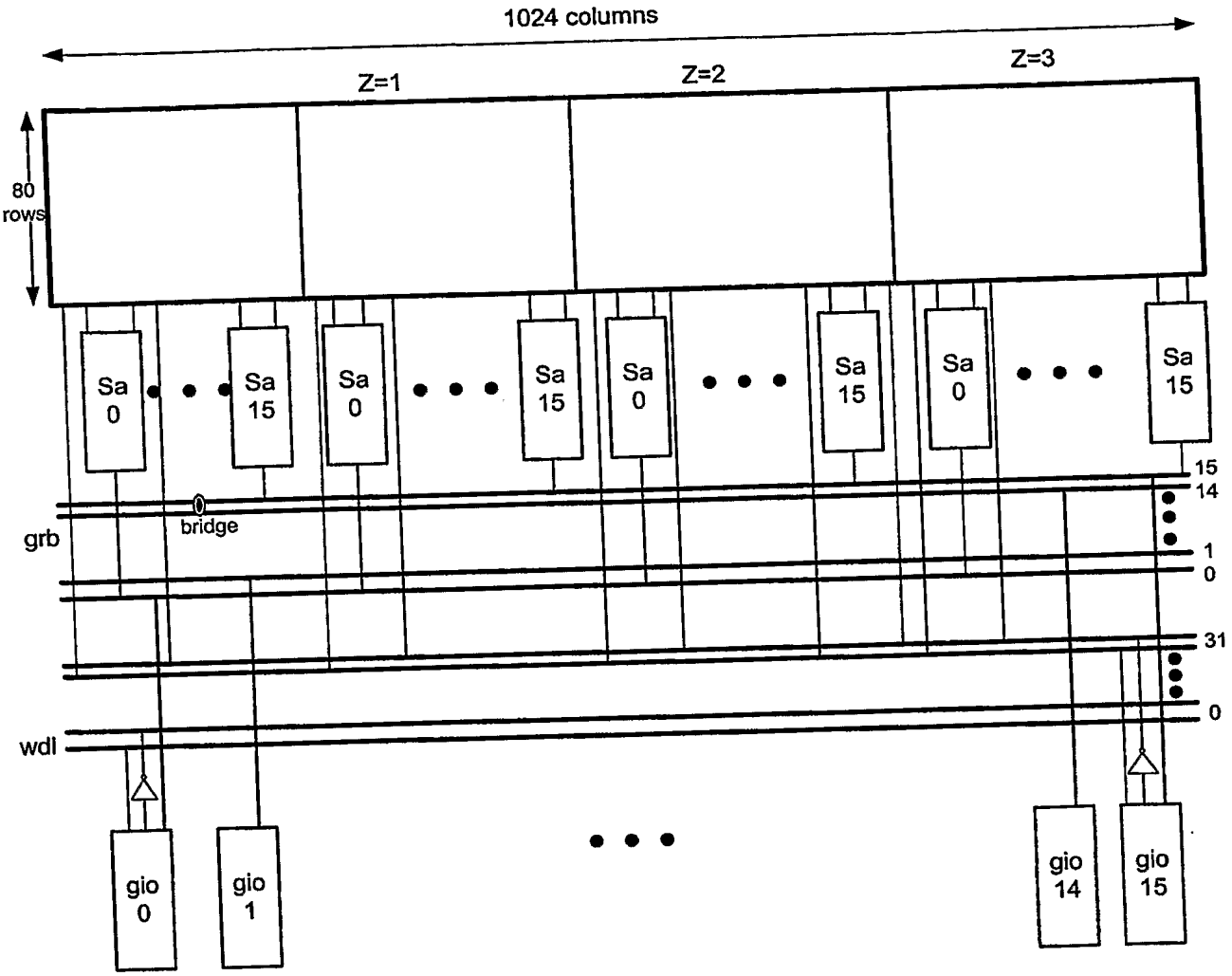

Figure 1: Multiple Z block architecture for semiconductor memories, showing a bridge between two read data lines.

This test escape occurs because the read data line R[i] becomes the neighbour of R[i+2] and R[i-2] instead of R[i+1] and R[i-1], while the write data line W[i] becomes the neighbour of W [i+2] and W[i-2] instead of W[i+1] and W[i-1]. In this case, the test pattern 00110011 or 11001100 will detect the bridge. To cover all the possible scrambling of the global read bus and the global write bus, we will run the data backgrounds shown in Table 1 (this is only the case of eight bits per word). However, applying these data backgrounds on unique memory position to save test time is not sufficient to detect resistive bridges at the global data bus. This is mainly due to the physical distribution of the global inputs/outputs through the global read bus and the global write bus and also the physical location of the Z blocks. When a resistive bridge is located near by the Z block 0 as shown on Figure 1, the resistive bridge may

escape the test with the mentioned data backgrounds if they are written and read out at the third Z block. This is mainly due to the physical location of the fifteenth global inputs/outputs, which is located near by the third Z block, and far away from the physical location of the defect. Figure 1 shows that the resistive bridge is located in between the read data lines R[15] and R[14] or in between R[15] and R[13] in case of scrambling, this defect will not be detected even when the test pattern 01010101 and 00110011 are respectively used at the third Z block. The read-out data will flow from the third Z block to the global outputs correctly. Depending on the defect location and the defect size (modelled by the resistive value of the bridge), the defect will only disturb the carried signal but will not change the logical behaviour of the data. Therefore, the defect will escape the test. Similarly, a second defect which may be located in between R[0] and R[1] or between R[0] and R[2] (in case of scrambling) will also escape the test if the correct test patterns are used at the Z block 0.

This test escape is due to many parameters that are: the number of Z blocks, the length of the metal lines, the defect location, the defect size and finally the physical location of the global inputs/outputs which are shared between all Z blocks and are not equally distributed through out the chip.

Moreover, applying these data background to all Z blocks will explode the test complexity and will highly increase the test time.

2. Disadvantages

The family of the march test are not covering the resistive bridges at the global read bus and the global write bus. The extension of the family of march test patterns to cover the bridging defects at these buses can be done by applying the data background shown in Table 1. However, the test complexity of the family of the march test will be highly increased, and also the test time depending on the number of bit per word and the memory size.

Applying a march test with a determined data background and the inverted data background will result to test escape and will highly increase the customer returns. Many resistive bridges at the global read bus and the global write bus will escape the test. This will lead to ship faulty products and may also cause a reliability issues, because the weak bridges that have no fault effect on the memory behaviour may become strong after many hours of use and then cause a faulty behaviour.

The resistive bridges at the global read bus and the global write bus are not easily detected by the family of the march test, unless the mentioned data background are taken into account. Combining the march test with the mentioned data backgrounds will dramatically increase the test algorithm complexity and test time.

3. Proposed solution

We propose a new way to apply the different data backgrounds needed to cover all resistive bridges at the global read bus and the global write bus. The solution will cover the resistive bridges at the global read and write buses and will also reduce the test complexity and therefore the test time. To increase the fault coverage and to reduce the test algorithm complexity, the data background of Table 1 (which should be modified depending on the number of bits per word) must be applied to all the Z blocks but not at all the memory positions. If we run the data backgrounds through all the Z blocks, we will cover all the physical location of the bridges. Selecting specified

memory addresses at each Z block is sufficient to cover the resistive bridges at the global data buses and will decrease the test complexity. The condition of crossing the global read bus to the global memory outputs from all the corners of the chip is verified. Similarly, the condition of crossing the global write bus from the global memory inputs is verified. Therefore, all the data paths from the global data bus to all Z blocks is verified. In this way, all resistive bridges are covered. The reason behind repeating the same data background four times at each bit column is to cover also the weak bridges not only at the global read bus and the global write bus, but also at the bit lines and the sense amplifiers. Actually, The needed data backgrounds must be written at all the Z blocks at least at one memory position. Usually, it is the highest memory position of the matrix to cover also some of the problem at the bit lines and the sense amplifiers. However, to cover the load issues of all the bit lines and to cover also all data paths of the memory, all bit columns must be tested at least for four times. This action is helping to cover the weak resistive bridges at the global data buses because many iteration are needed to sensitise the weak defects. This will result to run the mentioned data backgrounds four times for each bit column, and then for each Z block, as shown in Figure 2.

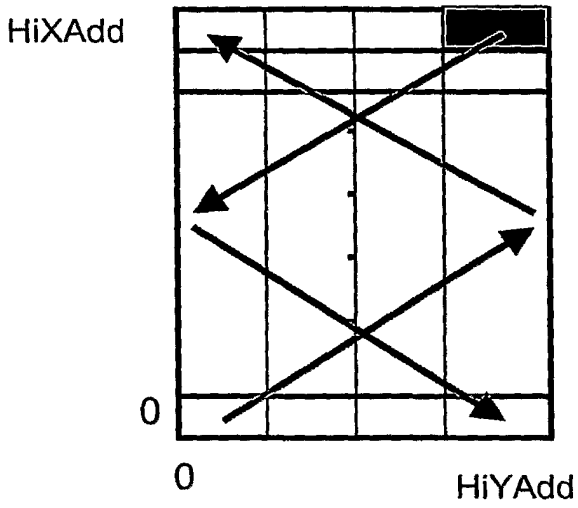

Figure 2: Test algorithm using different data backgrounds with multiple memory addresses (case of one Z block).

The new test algorithm comprises of running all the data backgrounds shown in Table 1 at the memory position shown in Figure 2. These test patterns must be repeated for each Z block. This is equivalent to walk in form of 2X on each Z block by testing all the bit columns and by selecting some of the rows. In this way, all the bit columns are tested four times with the mentioned data backgrounds. As we show in Figure 2, the matrix is divided into two Xs, the lower X and the upper X, which gives the physical addresses of the accessed memory positions. According to Figure 2, the mentioned data backgrounds are applied in selective diagonal way.

In case of Read-Only Memories (ROMs) organized by Z blocks, the global write bus does not exist, however, the global read bus must be tested with the same data

background explained in Table 1. This will help only for diagnosing the resistive bridge in the global read bus. For these memories, only consecutive read operations are allowed. The memory content of the ROM can not be changed because it is hard coded, therefore, the global read bus can be tested by reading the memory content that verify partially all the combination explained on the Table 1. A set of consecutive read operations may be combined to verify the data backgrounds in Table 1. Suppose that the pattern 01010101 described in Table 1 is not hard coded in the ROM. A combination of adjacent bits of 01 and 10 from different memory positions can be read out to test the global read bus. It has the same effect as reading the real pattern 01010101. Different memory positions may contains the test patterns 0111_1111, 1101_1111, 1101_0000, 1111_0100 and 0000_0001. This means that reading the pattern 01010101 will be substituted with 5 read operations. The same apply for the other test patterns. In case of multiple port SRAMs organized by Z blocks, it is sufficient to test the global read bus and the global write bus from one of the memory port where a read and write operations are allowed.

4. Advantages

This solution will highly increase the resistive bridge defect coverage at both the global read bus and the global write bus and it also takes into account the weak resistive defects. These defects may escape the test due to the physical location of Z blocks and the global inputs/outputs and also the defect size. These weak defects are also stressed by executing four iterations at each column bit for each Z block. These new test patterns are not only able to detect the resistive bridges at the global data buses but also allow to test all the bit lines and the sense amplifiers. The fact that all the Z blocks are tested with the mentioned data backgrounds which will cover all resistive bridge defects at the global read/write bus. This is because the data backgrounds cross theses buses from left to right and from right to left corners of the chip.

5. Background material

The background material herein is incorporated by reference in its entirety.

[1] A. J. van de Goor, "Testing semiconductor memories theory and practice", Gouda, The Netherlands, 1998.
[2] R. Dekker et al. " A realistic fault model and test algorithms for static random access memories", IEEE transactions on computers, C-9 (6), pp 567-572.
[3] M. Azimane, " New test methods to detect address decoder delay faults in ROM", TN7176, Sept 2001.